English Abstract of CN Publication No. 1235375A

A mounting structure of a semiconductor chip including a semiconductor chip 6 with a plurality of bumps 16, and a circuit substrate 3 with a plurality of output wires 11 and input terminals 12. In the press-bonding process, ACF 4 is used to join the semiconductor chip 6 and the circuit substrate 3 together so as to allow electrical conduction between the bumps 16 and the land parts of, for example, the output wires 11. A plurality of transfixion holes 10 are formed so as to be spread out in an area of the circuit board 3 surrounded by the land parts of the wires 11 and the terminals 12, and the excess ACF 4, present during the press-bonding, is allowed to escape through the transfixion holes 10, thereby preventing generation of a large internal stress in the ACF 4. This allows the IC 6 to be joined more reliably.

[19]中华人民共和国国家知识产权局

[51]Int. Cl[6]
H01L 23/00
G09F 9/35

[12]发明专利申请公开说明书

[21]申请号 99104085.6

[43]公开日 1999年11月17日

[11]公开号 CN 1235375A

[22]申请日 99.3.23 [21]申请号 99104085.6

[30]优先权

[32]98.3.24 [33]JP [31]76334/98

[32]98.10.8 [33]JP [31]287099/98

[71]申请人 精工爱普生株式会社

地址 日本东京都

[72]发明人 内山宪治

[74]专利代理机构 中国专利代理(香港)有限公司

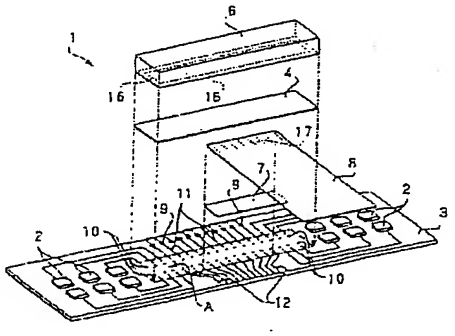
代理人 杨 凯 叶恺东

权利要求书2页 说明书13页 附图页数8页

[54]发明名称 半导体芯片的安装结构体、液晶装置和电子装置

[57]摘要

本发明的课题是在使用各向异性导电膜(ACF)等的粘接剂将半导体芯片安 装在基板上的安装结构体中防止在粘接剂中产生残留应力以提高电极端子间的 连接可靠性。该安装结构体包括具备多个凸点16的半导体芯片6和具备多条 输出布线11和输入端子12的电路基板3。在电路基板3中被布线11和端 子12的接合区部分包围的区域内分散地配置多个贯通孔10,使压接处理时 成为多余的ACF4通过这些贯通孔而逸出,由此来防止在ACF4中产生大 的内部应力。



ISSN1008-4274

专利文献出版社出版

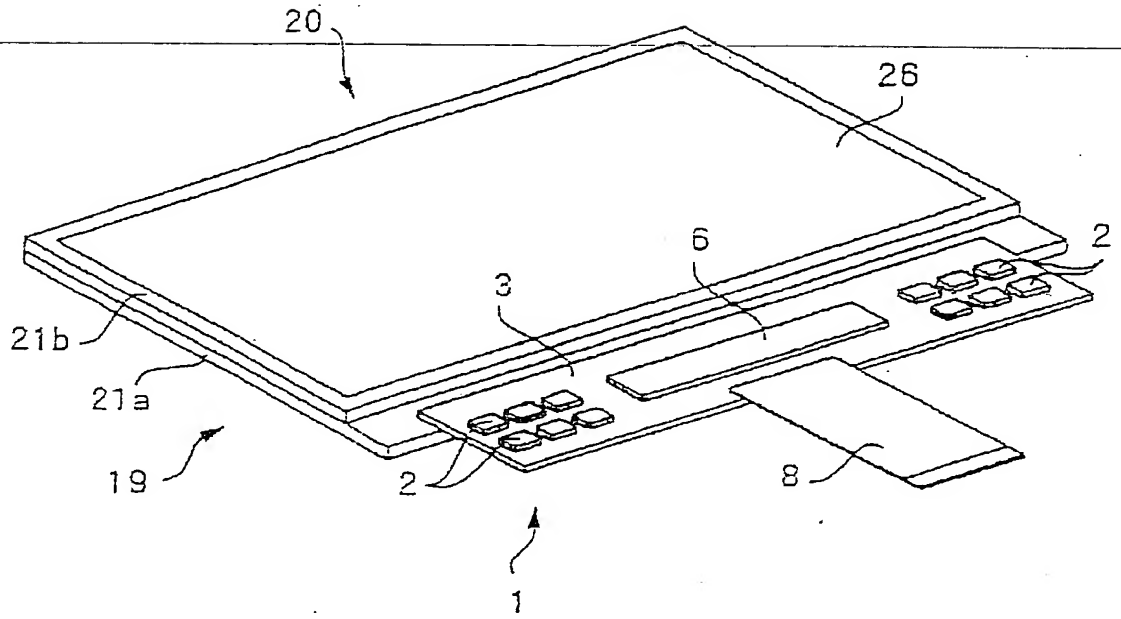


图 3

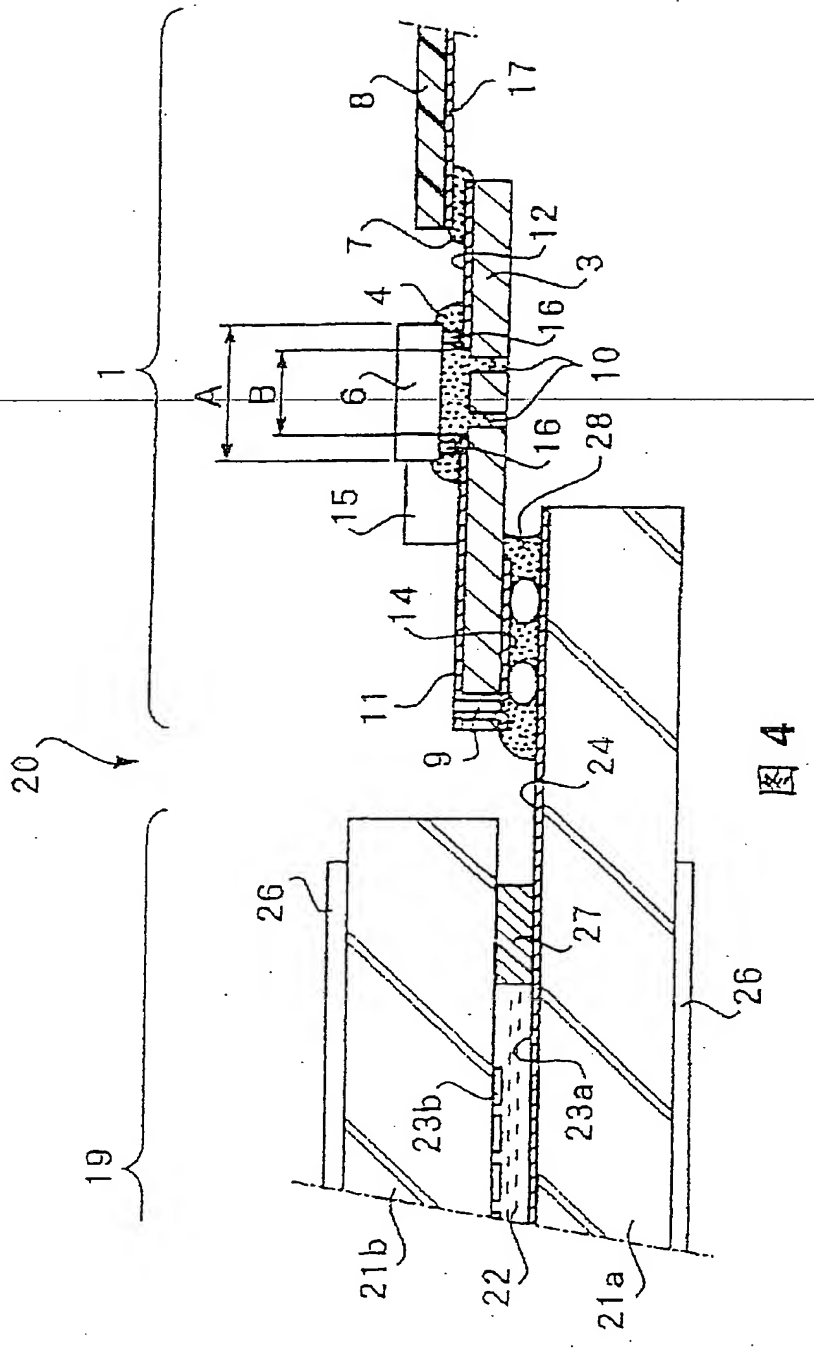


图 4